

# Sudipta Kundu

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## Contact Information

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**Current Status**    Ph.D. candidate, Department of Computer Science and Engineering  
University of California at San Diego, La Jolla, CA

**Citizenship**        Indian, Student Visa F1

## Research Interests

Program Analysis, Software Engineering, Software Verification,  
Concurrent System Analysis, System-Level Hardware Verification.

## Education

*Ph.D., Computer Science and Engineering*, in progress (expected Summer 2009)  
University of California at San Diego (UCSD), La Jolla, CA  
Thesis: *High-Level Verification of System-Level Designs*  
Advisers: Prof. Rajesh Gupta and Prof. Sorin Lerner  
GPA: 3.88/4.0

*5 Year Integrated Master of Science, Mathematics and Computing*, May 2004  
Indian Institute of Technology (IIT) at Kharagpur, India

Master Thesis: *Design and Optimization of an application specific Operating System*

Advisers: Prof. Anupam Basu and Prof. U. C. Gupta

Bachelor Thesis: *Assembler and Simulator for a subset of 8086 Assembly Language*

Adviser: Dr. Pawan Kumar

GPA: 9.12/10.0

Rank in the Department: 1<sup>st</sup>

## Honors

- *CAL-IT(2) Fellowship award*, 2004-05 from Department of Computer Sc. and Engg., UCSD.
- *Silver Medal*, 2004 from IIT, Kharagpur for being ranked first in the department.
- *Student Fellowship*, 17th International Conference on VLSI Design, Jan 2004, India.
- *J. C. Ghosh memorial prize*, 2003 from IIT Kharagpur for academic excellence.

## Research Experience

### Summer Internships

- 2008: *NEC Labs America, Princeton, NJ*; “Efficient Verification of Concurrent Programs using a Bounded Model Checking (BMC) Framework” under the supervision of *Dr. Malay Ganai*.
- 2007: *NEC Labs America, Princeton, NJ*; “Verification of SystemC Transaction Level Model (TLM)” under the supervision of *Dr. Malay Ganai*.
- 2006: *INRIA, Rennes, France*; “Compositional Modeling and Synthesis of Systems on a Chip” under the supervision of *Prof. Jean-Pierre Talpin*.
- 2005: *INTEL Corporation, Portland, OR*; “Dynamic Measurement of Available Bandwidth in a Heterogeneous Home Network”, under the supervision of *Narasimham Gadiraju*.

- 2004: *Communication Empowerment Laboratory, IIT Kharagpur*; “Porting of Embedded Linux and Application to the TI OMAP Platform”, under the guidance of *Prof. Anupam Basu*.
- 2002: *Centre for Internet Research, National University of Singapore (NUS)*; “Process Management of Embedded Linux” under the guidance of *Dr. A. L. Ananda*.

### Graduate Class Projects

- *Fall 2005*: Implemented test beds on Intel’s Mainstone with *Xscale pxa27x* processor for “Performance Comparison using Different Routing Metrics in Ad-hoc Wireless Networks”, under the guidance of *Dr. Tajana Simunic Rosing*.
- *Fall 2004*: Worked on “Improving Function and Array Support in SPARK, a parallelizing High-Level Synthesis Framework”, under the guidance of *Prof. Rajesh Gupta*.

### External Reviewer

*IEEE Transactions on Computer Aided Design.*  
*IEEE Transactions on Design Automation of Electronic Systems.*

## Publications

### Journal Papers

**Sudipta Kundu** and Sorin Lerner. Translation Validation in High-Level Synthesis. *In Submission*, 2009.

**Sudipta Kundu**, Sorin Lerner, and Rajesh Gupta. High-Level Verification. *IPSJ Transactions on System LSI Design Methodology*, 2009. (Invited Paper). *To Appear*.

### Conference Papers

Malay Ganai and **Sudipta Kundu**. Reduction of Verification Conditions for Concurrent System using Mutually Atomic Transactions. In *SPIN ’09: Proceedings of the 16th International SPIN Workshop on Model Checking of Software*, 2009. *To Appear*.

**Sudipta Kundu**, Zachary Tatlock, and Sorin Lerner. Proving Optimizations Correct using Parameterized Program Equivalence. In *PLDI ’09: Proceedings of the 2009 ACM SIGPLAN conference on Programming Language Design and Implementation*, 2009. *To Appear*.

**Sudipta Kundu**, Sorin Lerner, and Rajesh Gupta. Validating High-Level Synthesis. In *CAV ’08: Proceedings of the 20th international conference on Computer Aided Verification*, pages 459–472, Princeton, NJ, USA, 2008. Springer.

**Sudipta Kundu**, Malay Ganai, and Rajesh Gupta. Partial Order Reduction for Scalable Testing of SystemC TLM Designs. In *DAC ’08: Proceedings of the 45th annual conference on Design Automation*, pages 936–941, New York, NY, USA, 2008. ACM.

**Sudipta Kundu**, Sorin Lerner, and Rajesh Gupta. Automated Refinement Checking of Concurrent Systems. In *ICCAD ’07: Proceedings of the 2007 IEEE/ACM International Conference on Computer-Aided Design*, pages 318–325, Piscataway, NJ, USA, 2007. IEEE Press.

Gurashis Singh Brar, **Sudipta Kundu**, Pratik Worah, Susmit Biswas, Arijit Mukherjee, and Anupam Basu. OaSis: An Application Specific Operating System for an Embedded Environment. In *VLSI Design ’04: 17th International Conference on VLSI Design*, pages 776–779, Mumbai, India, 2004. IEEE Press.

### In Preparation

Frederic Doucet, **Sudipta Kundu**, Ingolf H. Krüger, R.K. Shyamasundar, and Rajesh Gupta. Compositional Design Methodology for Scalable Verification of System Design, 2009.

## Patents

Malay Ganai and **Sudipta Kundu**. Partial Order Reduction for Scalable Testing in System Level Design. *US Patent Pending*, 2008.

## Competition Participated

Developed a Chat Messenger and Server for Ideon 2001, the technology fest organized by IIT Kharagpur. National rank: 3<sup>rd</sup>.

Designed and Implemented a Verilog Logic Circuit Viewer for Ideon 2002, which takes in a structural Verilog program and displays graphically its logic circuit. National rank: 3<sup>rd</sup>.

## References

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System LSI and Software Verification  
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