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## JEFFREY NAMKUNG

### EDUCATION

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Sept. 2003-Present                      University of California                      San Diego, CA  
*Ph.D. student in Computer Engineering*  
GPA: 3.87  
Advisor: Rajesh Gupta

Aug. 1999-May 2001                      University of Illinois                      Urbana, IL  
*M.S. in Electrical Engineering*

- Master's Thesis – “An Event-Level Power Measurement Methodology and Analysis”
- Research Topics: low-power processors, computer networks, signal processing, image compression

Aug. 1995-May 1999                      University of Illinois                      Urbana, IL  
*B.S. in Computer Engineering*

- Edmund James Scholar

### WORK EXPERIENCE

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June 2005-Dec 2005                      Intel                      Santa Clara, CA  
**Graduate Intern**  
*Phase Analysis for multi-threaded workloads*

- Extended phase analysis for trace compression of MT-workloads on CMP systems
- Submitted paper to DAC entitled “*Workload Guided Sampling and Phase Synthesis for Efficient Simulation of Multi-threaded Workloads for Chip Multiprocessor Systems*”

*Content based image retrieval*

- Software engineering of content based image retrieval software
- Development of graphical user interface
- Aided in development and integration of various components from other team members

Jan. 2004-Present                      University of California                      San Diego, CA  
**Graduate Student Researcher**  
*Mixed Multi-scale Discrete Event Simulator Integration*

- Integration of multi-granular discrete-event simulators
- Integrated network simulator (NS-2), with System C and Instruction Set Simulator (SimpleScalar) for network embedded systems.

March 2005-June 2005                      University of California                      San Diego, CA  
**Teaching Assistant**  
*CSE 105: Automata Theory*

- Taught discussion sections, proctored exams, office hours, and grading

Sept. 2003-Dec. 2003                      University of California                      San Diego, CA

**Teaching Assistant**

*ECE 111: Advanced Digital Design*

- Aided students in HW/SW co-design, simulation, and synthesis of WEP encryption block for ARM based SoC
- Tools used: Synopsys Design Compiler and ModelSim

July 2000-March 2005                      Jet Propulsion Laboratory                      Pasadena, CA

**Member Engineering Staff**

*Hyperspectral Image Compression*

- Developed and implemented several hyperspectral image compression algorithms including seven integer wavelet transforms and various spectral prediction techniques
- Implemented Huffman encoding on transformed images with lossless compression rates of up to 4:1
- Implementing algorithms on an FPGA for high performance utilizing parallel computations not feasible in software
- Hardware/software partitioning via Xilinx Vertex 2 Pro FPGA which includes a PowerPC IP core

*Fault Tolerant Computing*

- Analyzed fault sensitivities architecturally on a PowerPC based system
- Integrated a software fault injector (SWIFI) into several Mars Rover based applications including stereo-image processing, image-mapped navigation, and a suite of traverse science modules
- Demonstrated software fault-tolerance techniques on the Rocky 8 rover running a stereo-image processing and navigation subset of the rover software

*Non-volatile Memory Endurance and Reliability Tester*

- Aided in the design and implementation of a low-cost FPGA-based non-volatile memory tester for endurance and reliability characterization
- First authored results of research in a conference paper which was presented at the Non-volatile Memory Technology Symposium in 2002

*Power-Aware Performance Computing*

- Designed and implemented a complete power measurements and performance test bench utilizing a single board computer running VxWorks and the Deep Space 1 flight software suite
- Profiled energy/power consumption of a Motorola PowerPC 750 at the instruction-level, event-level, and OS task-level (Deep Space 1 tasks).
- Results used by University of California – Irvine, University of Notre Dame, and State University of New York – Suny to perform compiler and architectural power-aware optimizations

Aug. 1999-May 2000                      University of Illinois                      Urbana, IL

*Teaching Assistant for the Department of Electrical and Computer Engineering*

- Taught ECE311 – Microcomputer laboratory for two semesters

- Design and verification of embedded systems utilizing FPGA's, embedded microprocessors, SCSI protocols, and NTSC Video protocols
- Aug. 1999-May2000                      University of Illinois                      Urbana, IL  
*Research Assistant*
- Implemented several branch prediction schemes including gshare, Agree, and various two-level prediction schemes
  - Benchmarked implemented branch predictors with the SPEC95 benchmarks using the SimpleScalar instruction-set simulator
  - Implemented a two-level cache simulator
  - Aided in the review of conference paper submissions

## PUBLICATIONS

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- J. Namkung. "An Event-level Power Measurement Methodology and Analysis," Master's Thesis, May 2001.
- J. Namkung. "Reliability and Endurance of FRAM," in the Proceedings of the 3<sup>rd</sup> Annual Non-Volatile Memory Technology Symposium, Honolulu, HI, Nov. 4, 2002.
- P. Kogge, J. Namkung, N. Aranki, N. Toomarian, K. Ghose. "Characterization of Future Deep Space Computing Loads" to appear in the Proceedings of the International Conference on Space Mission Challenges for Information Technology (SMC-IT).

## SKILLS

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### *Programming Languages*

- C, C++, JAVA, VHDL, Verilog, System C, NesC, Perl, LISP, OpenGL, TCL/TK, Sed, Awk, MatLab, LaTeX

### *Operating Systems*

- VxWorks, Windows (all versions), UNIX, LINUX, TinyOS

### *Tools*

- Xilinx ISE tools, Xilinx EDK tools, ModelSim, Synopsys Design Compiler, GNU tools, Microsoft Office, Visio, OrCAD, UNIX environment/shell scripts, Network Simulator (NS-2), TOSSIM, SimpleScalar.