When you look at the share of semiconductor content in electronic systems, two major inflection points clearly stand out: the PC in the late 1980s, and networking in the late 1990s—each contributing an approximate 5% jump in the IC content of all electronic systems. Semiconductors now account for 19% of the more than $1 trillion electronic systems industry. By some accounts, the industry is approaching another inflection point—the growth in wireless and consumer electronics—which has the proliferation potential of another 10%. Perhaps nothing symbolizes this proliferation of microelectronic components better than the ubiquitous cell phone, which is evolving into a platform for converged media access, entertainment, and more.

As a platform, the cell phone is a semiconductor company’s dream machine: Get your IC component on this platform, and you instantly have a market for your part that counts into millions of units. No wonder the cell phone and mobile handset industry is currently experiencing a tremendous surge of innovation in essentially all its components—from digital cameras, application and baseband processing, and RF front ends to power supply and display technologies.

Obviously, space is a premium in this platform. SoC integration has been a theme in most mobile platforms, from companies such as Texas Instruments, Motorola, Qualcomm, STMicroelectronics, and Intel. Pretty much all digital components, from processors to peripheral interfaces, have converged into highly integrated SoCs; multiple radios are also converging into single components. But SoC integration can only go so far before it is limited by the cost constraints associated with the heterogeneous devices on a single substrate. Highly specialized memory parts, including Flash, SDRAMs, and PSRAMs, are often thinned down and combined into multichip packages. Not only is this technologically easier to put together—it reduces the typical SoC integration problems related to yield and reliability—but it is also financially beneficial: For a fabless semiconductor company, components provide an easier revenue stream than do the IP blocks required for building SoCs. All these factors make a strong case for the vertical stacking, or 3D integration, of semiconductor components.

3D integration techniques, from wafer stacking to transistors along trench walls in 3D circuits, have existed since the 1980s. Recently, however, new products and platforms—enabled by substantial increases in processing, communications, and storage—have driven major advances in this area. To be sure, 3D integration has its own challenges—from worsening heat removal to EDA tools and tool flows supporting such design styles. Our guest editors, Kevin Nowka and Sachin Sapatnekar, have put together a comprehensive special issue on 3D integration that consists of seven well-written articles. These articles address issues ranging from architectural design, performance analysis, and interconnect design to physical design for 3D ICs and system on package.

This issue also includes a special section of articles selected from the International Test Conference (which takes place this November in Austin, Texas). These articles were selected based on the program committee’s nominations as significant advances in areas of interest for ITC. D&T’s ITC liaison, Scott Davidson, has diligently selected three articles that address identifying defective chips using wafer-level test data, test response compaction in the presence of unknown logic values, and methods to reduce yield loss through innovations in ATPG. Thus, this issue explores both design and test topics, and I hope you will find it a compelling and enjoyable read.

This is the last issue that I will oversee as editor in chief. Over the past four years, D&T has progressed; the editorial board reflects strong design and test components, and it includes a very active and capable set of editors and contributors from the EDA domain. EDA is the necessary third dimension to the range of design and test capabilities required for advancing microelectronic sys-
tems—on chip or in package. With that in mind, D&T has built and sustained a wonderful relationship with the prime EDA forum, the Design Automation Conference, over the past six years. D&T is also a proud and founding organization member of the new IEEE Council on Electronic Design Automation (CEDA). Together, D&T and CEDA plan to build a community of researchers that will lie at the heart of microelectronic advances.

Over the past four years, D&T has also undergone many changes, from the layout of the magazine to the rationalization of response time on all submissions—regular and special issue. I am very proud of our editorial board and its responsiveness to our contributors; the board has developed a strong culture of thoroughly vetting all special issue proposals. D&T’s average turnaround for submitted manuscripts (from submission to first decision) is 78 days, with a submission-to-acceptance average turnaround of 145 days. All published articles in D&T are independently and thoroughly peer reviewed, with an acceptance rate that hovers around 20% to 25%.

Reflecting the increase in community participation and selectivity, the magazine’s impact factor has doubled over this four-year period, ahead of its competitors and second only to Computer. Electronic readership is a growing component of our general readership, with each article seeing on average 175 downloads from IEEE Xplore. Thanks to the able leadership of Angela Burgess, Dick Price, and Janet Wilson, D&T has seen a positive and growing bottom line since 1999, ensuring the magazine’s long-term viability and responsiveness to our community of contributors.

The EIC search committee has concluded its deliberations conducted over the year. Given the strong community of contributors that D&T has built over the past two decades, this search, though extensive, was relatively easy. Of the three finalists, any one could have filled this role wonderfully, and I am happy to report that all three will be associated with the magazine in one capacity or another. Our incoming EIC is no stranger to D&T: Kwang-Ting (Tim) Cheng has been associated with D&T for eight years, the past six as its associate editor in chief. Tim brings deep technical talent and an enormous breadth of leadership experience to the EIC position. With Tim at its helm, I am confident that D&T has a bright future.

As you can tell, I have had tremendous fun all these years as EIC. My thanks go to a wonderful editorial staff—Anna Kim and Kimberly Banker—and a great set of volunteers, contributors, and readers. D&T certainly couldn’t have done without your participation!